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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,641	12/04/2003	Ming-Dou Ker	6720.0117-00	6205

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EXAMINER
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BENENSON, BORIS

ART UNIT	PAPER NUMBER
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2836

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05/02/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

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<b>Office Action Summary</b>	<b>Application No.</b>		<b>Applicant(s)</b>	
	10/726,641		KER ET AL.	
	<b>Examiner</b>		<b>Art Unit</b>	
	Boris Benenson		2836	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 02 March 2007.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 4, 28, 31, 44 and 48-69 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) 28 and 44 is/are allowed.
- 6) ☒ Claim(s) 4, 31 and 48-69 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 September 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

***Detailed Actions***

1. Amendment received on 03/02/2007 is entered.  
Claims 4,28,31 and 44 are amended.  
Claims 1-3, 5-27, 29-30, 32-43, 45-47 are cancelled.  
New Claims 48 - 69 are entered.  
Claims 4, 28, 31, 44, and 48-69 are pending in the Application.

***Response to the arguments***

2. Applicant's arguments have been considered, but they are  
mote due new reasons of rejection.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs  
of 35 U.S.C. 102 that form the basis for the rejections under  
this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or  
a foreign country or in public use or on sale in this country, more than one  
year prior to the date of application for patent in the United States.

3. Claims 4 and 31 are rejected under 35 U.S.C. 102(b) as  
being anticipated by Faraci (4,985,870). Faraci disclosed an  
Apparatus For Connecting Electronic Modules Containing  
Integrated Circuits And Backup Batteries. An interface device  
includes a circuit board (Pos. 12) with a connector (22) formed  
on the board with a plurality of contact first members -

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metallic connection traces (24) of a first length, including a first end connected to the board and a second end (close to the board edge) to connect to an external device (29) and two second contact members (32 and 34) of a second length greater than the first length, wherein a first of two second contact members (32) is connected to a first voltage line (VSS or ground) and a second of two second contact members (34) is connected to a second voltage line (VCC). The second contact members (32 and 34) contact the external device prior to first contact members contacting the external device. "In operation, when the module 10 is inserted into the card edge connector 28, the metallic connection traces 32 and 34 make physical and electrical contact with their respective spring contacts 30 before the other metallic connection traces are contacted. Similarly, when the module 10 is disconnected from the card edge connector 28, the metallic connection traces 32 and 34 remain in electrical contact with their respective spring contacts 30 after the other metallic connection traces have been disconnected from their respective spring contacts" (Col.4, Lines 12-22).

4. Referring to Claim 31, the method is anticipated by structure of apparatus of Claim 4.

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***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 48-53 rejected under 35 U.S.C. 103(a) as being unpatentable over Faraci (4,985,870) in view of Banakis et al. (5,653,596) and Taylor et al. (5,677,511). Faraci disclose an Apparatus For Connecting Electronic Modules Containing Integrated Circuits And Backup Batteries, wherein a circuit board includes a plurality of first contact lines (Pos.24) having ends extending toward, but not reaching an edge of the board and two second contact lines having ends extending to the edge of the board. One of the second contact lines provided connection to a VCC power source and another second contact line provided connection to ground (VSS). Faraci disclose a third contact line formed adjacent a periphery of the board and having a first and second ends extending to the edge of the board. Banakis et al. teach a Grounding System For PC Cards. Banakis et

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al. teach two grounding terminals (Fig.1, Pos. 32) each of them comprising two grounding pins (Pos. 40). Banakis et al. teach "In particular, the ground terminals are arranged and coupled to the logic or common ground circuit means on main printed circuit board 14 to provide a low impedance ground return" (Col. 5, Lines 27-30). Neither Faraci nor Banakis et al. teach location of grounding trace on the board. Taylor et al. teach Overmolded PC Board With ESD Protection And EMI Suppression. Taylor et al. teach "a ground trace 12 travels around the outer perimeter 18 of the PC board 11 surrounding the active regions 13" (Col.4, Lines 30-32). Taylor et al. do not teach how ground trace is connected to a board connector. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Faraci with teachings of Banakis et al. and Taylor et al. and create more than one elongated contact for ground connection on opposite ends of connector as teach Banakis et al. and provide peripheral grounding trace of Taylor et al. connected to grounding contacts on opposite ends of connector, because it will provide a low impedance ground return according to Banakis et al. and protection against both electro-static discharge (ESD) and electro-magnetic interference (EMI) according to Taylor et al. It would have been obvious to one of ordinary skill in the art at the time the invention was made to

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have modified Faraci and have more than one elongated contact (second contact lines) for connection to a power source, if the circuit board requires connection to more than one voltage level such as VCC and VDD or a positive and a negative voltages, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ.

6. Claims 54-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ziemkowski (6,804,119) in view of Samela et al. (6,220,873). Ziemkowski disclosed Method And Edge Connector Providing Electrostatic Discharge Arrest Features And Digital Camera Employing Same. An apparatus (Fig. 1, Pos. 20) comprises a circuit board (Pos. 10) including a plurality of first contact lines (Pos. 14) having ends disposed at a first distance from an edge of the board, a second contact line - ground contact (Pos.12) having an end disposed at second distance from the edge of the board, wherein the second distance is shorter than the first distance, and a third contact line - power contact (Pos. 13) having an end disposed at a third distance from the edge of the board. Ziemkowski did not disclose at least one second contact line being disposed between two lines of the plurality of first contact lines. (Applicants did not disclose

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significance and advantage of such arrangement). Samela et al. teach a Modified Contact Traces For Interface Converter. Figures 4A and 4B show variety of contact lines adapted to be connected to external device through a socket (Pos. 710). A male connector shown on upper part of Figure 4A indicates at least one contact line with shorter distance from an edge (Pos. 545) of a board (Pos. 546) being disposed between two contact lines with longer distance from the edge. Figure 4B, which shows the bottom of the board, where displays contact lines that extends to the edge of the board. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Ziemkowski with teaching of Samela et al. and dispose at least one second contact line between two lines of plurality of first contact lines, because such a placement will enable a designer to adjust connector to a topography of a circuit board.

A method of Claim 60-64 is anticipated by structure of apparatus.

7. Claims 65-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sausen (6,626,6820 in view of Shuey (6,494,734). Sausen disclosed an Integrated Circuit Device Socket for "testing of semiconductor devices during manufacturing" (Col. 1, Lines 14-15). The device comprises a board (Figs 1A-1C, Pos 106) having a surface with a set of pogo-



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pins (Pos. 108). Sausen did not disclose at least one pin having length longer than the other pins. Shuey teaches a High Density Electrical Connector Assembly. The assembly comprises an insulative body portion (Fig. 1C, Pos. 12) with a plurality of pins of a first length (Pos. 14) and a guide pin (Pos. 16) of second length longer than the first length. Shuey teaches "The ground contacts which extend from the first connector are longer than the signal contacts so the ground contacts engage respective conductors in the mating electrical connector prior to the signal contacts engaging their respective conductors in order to discharge electrostatic charge to a chassis ground" (Col. 2, Lines 6-11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Sausen with teachings of Shuey and provide a ground pin with length longer than the signal contacts, because it will, as teaches Shuey, discharge electrostatic charge to a chassis ground.

***Allowable Subject Matter***

8. Claims 28 and 44 are allowed.

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**The following is an examiner's statement of reasons for allowance:**

9. Independent Claims 28 and 44 are allowable because none of the prior art of record disclose a detecting system or a method of providing electrostatic discharge protection in a detecting system for integrated circuits comprising a second board with a plurality of first contact points formed on a first surface of the second board and a plurality of a second pins formed on a second surface of the second board in combination with the other claim limitations.

**Contact information**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Boris Benenson whose telephone number is (571) 272-2048. The examiner can normally be reached on M-F (9-6).


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Boris Benenson  
Examiner  
Art Unit 2836

B.B.

 4/30/07

**MICHAEL SHERRY**  
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